IN THE CLAIMS

1. – 28. (Canceled)

29. (Previously Presented) A Substrate processing system which sequentially performs a plurality of processes on a plurality of substrates according to predetermined process procedures, comprising:

a plurality of modules into and out of which a substrate is transferred;

a substrate transfer mechanism which transfers said substrate between said modules; and

a control section which controls said substrate transfer mechanism in such a way as to perform a substrate process of a first lot including a plurality of substrates to be transferred in a first transfer flow with respect to said plurality of modules, and subsequently perform a substrate process of a second lot including a plurality of substrates to be transferred in a second transfer flow different from said first transfer flow with respect to said plurality of modules,

said control section including:

a transfer control table in which a transfer schedule representing a relationship between a transfer timing of the substrate and said modules into and out of which that substrate is transferred is stored in each of the substrate process of said first lot and the substrate process of said second lot, and which comprises a two-dimensional table including a time axis along which transfer timings at which a transfer operation of said substrate is performed in a predetermined cycle is set, and a transfer flow axis along which said modules into and out of which said substrate is transferred are laid out; and

a controller including a function of generating said transfer schedule of a plurality of substrates in a unit of a lot on said transfer control table by setting identification information of each of said substrates which is transferred into and out from said modules with respect to a cell to be specified by designating a specific one of said transfer timings and a specific one of said modules in said two-dimensional table, a function of moving all of said cells included in said transfer schedule of the substrate process of said second lot ahead in a direction of said time axis

within a range over which contours of figures constituted by said cells included in said transfer schedules of the respective substrate processes of said first lot and second lot set on said transfer control table do not interfere with each other, and a function of controlling said substrate transfer mechanism based on said transfer schedule read from said transfer control table at every said transfer timing.

30. (Previously Presented) A substrate processing system which sequentially performs a plurality of processes originating from resist coating and development after resist exposure on a plurality of semiconductor substrates according to predetermined process procedures, comprising:

a plurality of process modules which perform resist coating, and development after resist exposure on the semiconductor substrate, and a hydrophobic process, a heating process, a cooling process, and a holding process on the semiconductor substrate;

a substrate transfer mechanism which transfers the semiconductor substrate between said plurality of modules; and

a control section which controls said substrate transfer mechanism in such a way as to perform a substrate process of a first lot including a plurality of substrates to be transferred in a first transfer flow with respect to said plurality of modules, and subsequently perform a substrate process of a second lot including a plurality of substrates to be transferred in a second transfer flow different from said first transfer flow with respect to said plurality of modules,

said control section including:

a transfer control table in which a transfer schedule representing a relationship between a transfer timing of the semiconductor substrate and said modules into and out of which that semiconductor substrate is transferred is stored in each of the substrate process of said first lot and the substrate process of said second lot, and which comprises a two-dimensional table including a time axis along which transfer timings at which a transfer operation of said substrate is performed in a predetermined cycle is set, and a transfer flow axis along which said modules into and out of which said substrate is transferred are laid out; and

a controller including a function of generating said transfer schedule of a plurality of semiconductor substrates in a unit of a lot on said transfer control table by setting identification information of each of said semiconductor substrates which is transferred into and out from said modules with respect to a cell to be specified by designating a specific one of said transfer timings and a specific one of said modules in said two-dimensional table, a function of moving all of said cells included in said transfer schedule of the substrate process of said second lot ahead in a direction of said time axis within a range over which contours of figures constituted by said cells included in said transfer schedules of the respective substrate processes of said first lot and second lot set on said transfer control table do not interfere with each other, and a function of controlling said substrate transfer mechanism based on said transfer schedule read from said transfer control table at every said transfer timing.

31. (Previously Presented) The substrate processing system according to claim 29 or 30, wherein said controller further comprises a function which, when said transfer schedules of said first and second lots are set in said transfer control table in such a way that transfer recipes comprised of a combination of said modules and a transfer order of the substrate between said modules become equal to each other, sets said transfer schedule ahead for each of said modules in said transfer recipe.

32. (Previously Presented) The substrate processing system according to claim 29 or 30, wherein said control means further comprises a function which, when said transfer schedule of said first and second lots is set in said transfer control table in such a way that transfer receipts comprised of a combination of said modules and a transfer order of the substrate between said modules become equal to each other, intentionally delays a start timing of said transfer schedule of said second lot from an optimal start timing in such a way that a transfer in/out time to a specific one of said modules becomes equal for all the substrates of said succeeding lot.